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# Theory and Operation of Cold Field-effect Transistor (FET) External Parasitic Parameter Extraction

**by Benjamin D. Huebschman, Pankaj B. Shah, and Romeo Del Rosario**

**ARL-TR-4812** **May 2009**

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**Benjamin D. Huebschman, Pankaj B. Shah, and Romeo Del Rosario**
**Sensors and Electron Devices Directorate, ARL**

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**14. ABSTRACT**
The design of monolithic microwave integrated circuits (MMIC) is dependent on the ability to generate accurate device models. Prior knowledge of the external parasitic components is required to determine the small-signal model of the intrinsic device. In this report, we describe a technique and its implementation for extracting external device parasitics. The term cold field-effect transistor (FET) refers to measurements taken when the drain is at the same voltage as the source.

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## 1. Introduction

Existing semiconductor models are based primarily on modeling the active components of the intrinsic device (*1*). The design of monolithic microwave integrated circuits (MMIC) is dependent on the ability to generate accurate device models. In order to accurately model the intrinsic device, one needs a mechanism for extracting external parasitics. A well-known procedure for measuring external parasitics has been implemented with a modification (*1–3*). The results observed from using the extraction technique suggest that it is a reliable method for determining parasitic elements.

## 2. Theory

The difficulty in determining the component values of the equivalent circuit model of either a large-signal model or a small-signal model comes from ambiguity. For the purposes of this report, the term ambiguity, in the general case, refers to a calculated result that may result from several different inputs. In the specific case, ambiguity refers to a set of scattering parameters (S-parameters) that could be the result of different equivalent circuits or multiple instantiations of a single equivalent circuit using different sets of component values. The key to eliminating ambiguity and solving for a single unique solution is being able to perform experiments capable of isolating different parts of the circuit model so that they can be measured separately. This is done by applying a bias to a device that causes it to behave in a predictable manner. Outside of the normal operating regime of the device, a high electron mobility transistor (HEMT) can be forced to behave as either a short circuit or an open circuit. Figure 1 shows the model for the external parasitics that is used in this report and the equivalent circuit models currently under development at the U.S. Army Research Laboratory (ARL) (*1*).

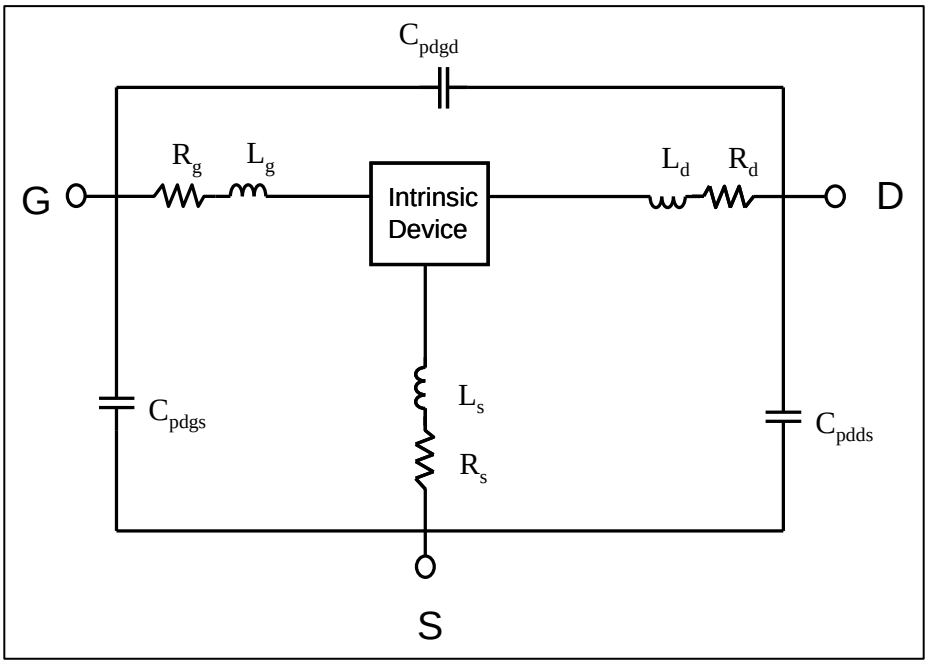


Figure 1. External parasitic equivalent circuit model.

The intrinsic device model is not relevant to the topic of this report and as such is treated as a black box. During the cold field-effect transistor (FET) measurements, the source and the drain are both held at zero volts. When biased in this manner, the device behaves like a diode.

## 2.1 Reverse Bias: Shunt Parasitic Capacitor Extraction

The device is reversed biased by setting the drain and source to zero volts and applying a negative voltage to the gate. When the device is reversed biased, the intrinsic device small-signal low frequency behavior can be modeled as an open circuit. In this case the diode is reverse biased. This setup allows the equivalent circuit model to be represented as a set of capacitors in parallel, as shown in figure 2.

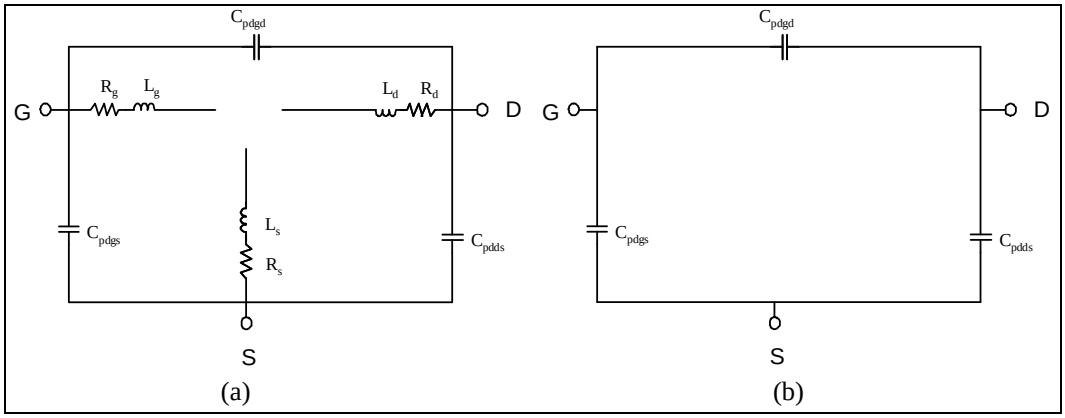


Figure 2. (a) Simplified equivalent circuit model of the reverse biased device and (b) with series components removed.

The circuit then becomes a three-terminal system connected by shunt capacitors. The equivalent Y-parameter model is shown in figure 3 (*4*).

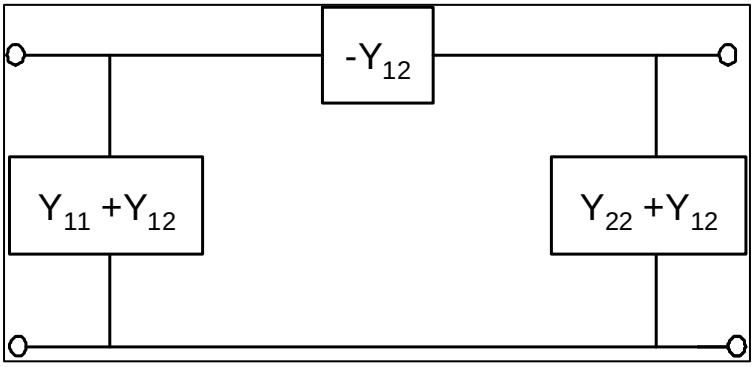


Figure 3. Admittance matrix equivalent circuit model.

The procedure for calculating the parasitic capacitances is shown below:

1. Apply a sufficiently negative bias to the device to pinch off the gate and drain.
2. Measure the S-parameters of the device.
3. Convert the S-parameters into admittance parameters.
4. Calculate the parasitic capacitances using the admittance parameters.

Equations 1–3 are used to calculate the parasitic capacitance for a given set of admittance parameters:

$$Cpgd = \mathrm{Im}\left(\frac{-Y_{12}}{\omega}\right) \tag{1}$$

$$Cpgs = \mathrm{Im}\left(\frac{Y_{11}}{\omega}\right) + \mathrm{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{2}$$

$$Cpds = \mathrm{Im}\left(\frac{Y_{22}}{\omega}\right) + \mathrm{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{3}$$

### 2.2 Forward Bias: Series Parasitic Capacitor Extraction

The procedures for extracting the series parasitic component values from the forward-biased device are analogous to those for the reversed-biased device but are more complicated and include several additional considerations. When the device is forward biased, the intrinsic device behaves like a short circuit. Measurement has shown that at high frequencies, a residual gate capacitance is present on the device and must be included in the model when extracting the parasitics. Figure 4 shows the model used to extract parasitics when the device is forward biased.

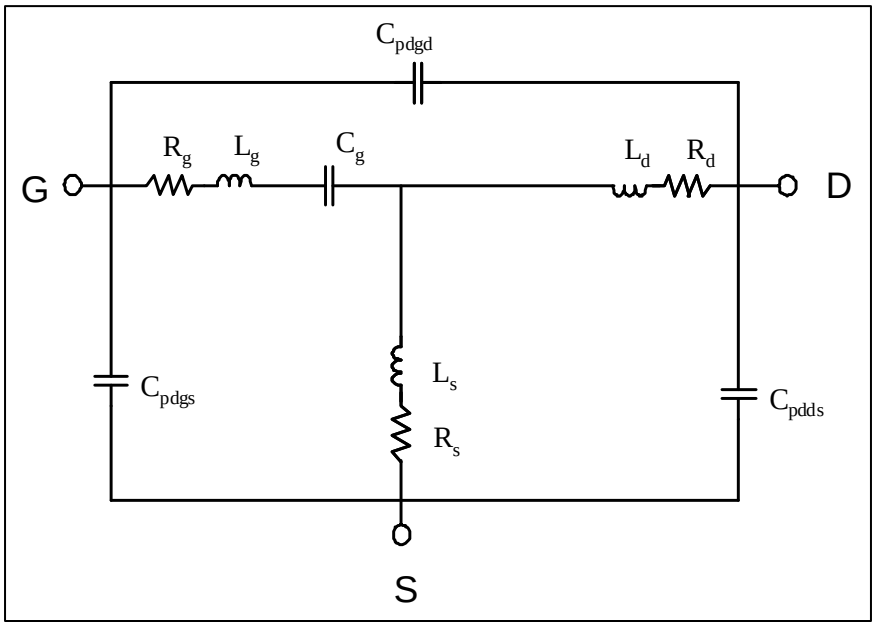


Figure 4. High frequency model of the forward-biased device.

The procedure for calculating the parasitic capacitances is as follows:

1. Apply a positive voltage to the gate to drive sufficient current through the device to put the diode into the “on” state but not enough current to damage the device.
2. Measure the S-parameters of the device.
3. Convert the S-parameters to Y-parameters.
4. Subtract the shunt parasitic capacitances.
5. Convert the S-parameters to Z-parameters.
6. Calculate the component values of the series elements.

In step 4, the admittance of the shunt capacitors are subtract from the extrinsic Y-parameters. The equations used for subtracting the Y-parameters are shown below:

$$Y_{11}' = Y_{11} - i\omega(Cpgs + Cpgd) \tag{4}$$

$$Y_{22}' = Y_{22} - i\omega(Cpds + Cpgd) \tag{5}$$

$$Y_{21}' = Y_{21} + i\omega\, Cpgd \tag{6}$$

$$Y_{12}' = Y_{12} + i\omega\, Cpgd \tag{7}$$

Following this, the admittance parameters with the parasitic capacitances removed are converted into impedance parameters. The equivalent circuit with the parasitic capacitance removed is shown in figure 5.

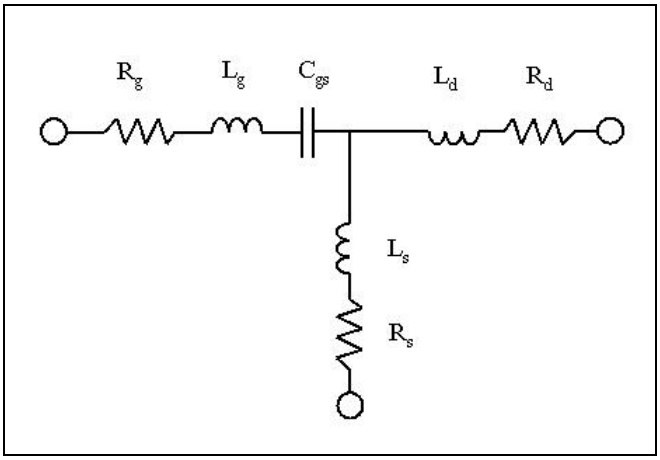


Figure 5. High frequency model of the forward-biased device with parasitic capacitances deembeded.

This model shows a three-terminal passive device. A well-known technique for determining the Z-parameters of such a system is shown in figure 6 (*4*).

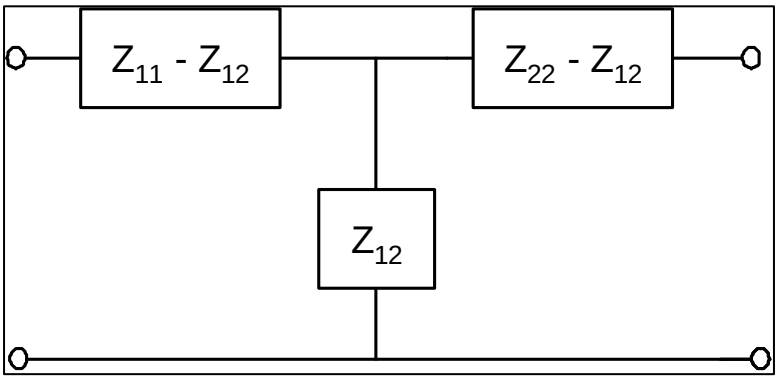


Figure 6. Impedance matrix equivalent circuit model.

From this, we can determine the impedance parameters of the model. Equations 8–10 show how to calculate the impedance parameters of the model in figure 5 (*2*):

$$z_{11} = R_g + R_s + j\omega(L_g + L_s) - \frac{j}{\omega C_{gs}} \tag{8}$$

$$z_{12} = z_{21} = R_s + j\omega L_s \tag{9}$$

$$z_{22} = R_d + R_s + j\omega(L_d + L_s) \tag{10}$$

Based on these equations, the parameter values can be calculated:

$$R_s = \mathrm{Re}(z_{12}) \tag{11}$$

$$R_g = \mathrm{Re}(z_{11}) - R_s \tag{12}$$

$$R_d = \mathrm{Re}(z_{22}) - R_s \tag{13}$$

$$L_s = \frac{\mathrm{Im}(z_{12})}{\omega} \tag{14}$$

$$L_d = \frac{\mathrm{Im}(z_{22})}{\omega} - L_s \tag{15}$$

$$L_g = \frac{\mathrm{Im}(z_{11})}{\omega} - L_s + \frac{1}{\omega^2 C_{gs}} \tag{16}$$

The term $C_{gs}$ must be determined by a separate procedure. There are several useful techniques for calculating $C_{gs}$. One can calculate $C_{gs}$ using a polynomial fit function on the reactive component of the impedance. We have developed a technique that uses differentiation to isolate elements that have different frequency dependence. Others have used knowledge of the fabrication process to estimate $C_{gs}$. This component can also be determined by examining the resonance properties of that branch of the T junction.

## 3. Measurement Procedure and Software Operation

We implemented the cold FET method in the Radio Frequency (RF) Test lab. Figure 7 shows a graphic representation in flow chart form of the programs used to perform the cold FET measurement.

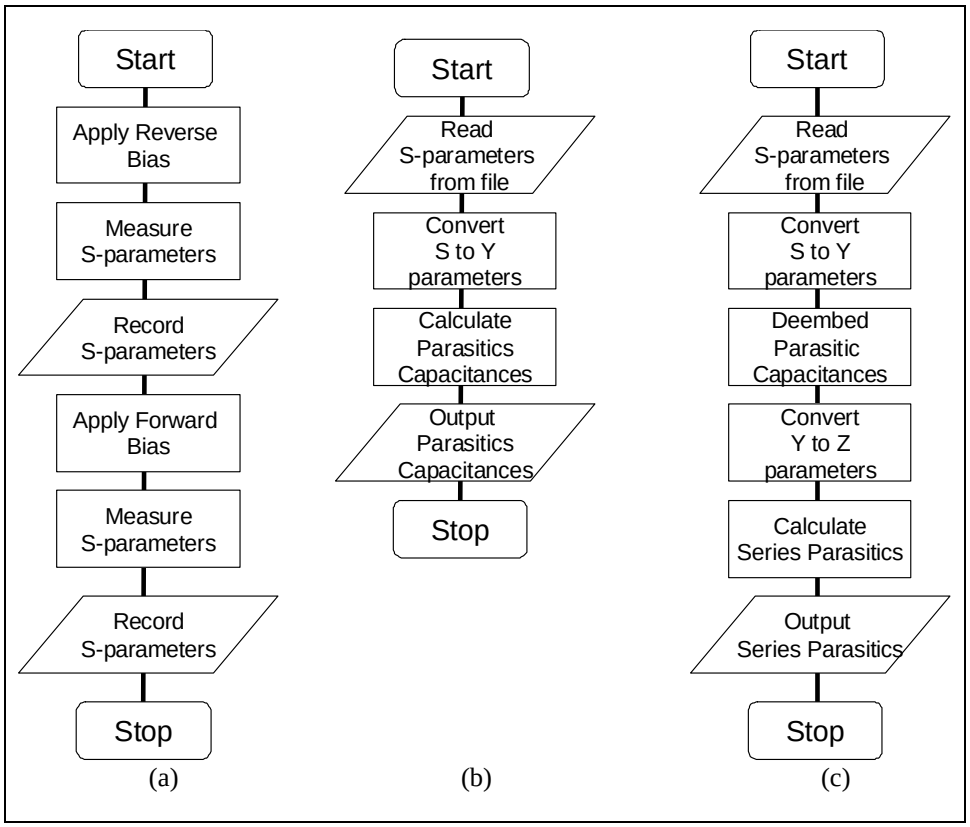


Figure 7. Flow chart for cold FET programs (a) instrument control (b) parasitic capacitance calculation (c) series parasitic calculation.

### 3.1 System Hardware

We used the ARL load pull system depicted in figure 8 to perform the cold FET measurements.

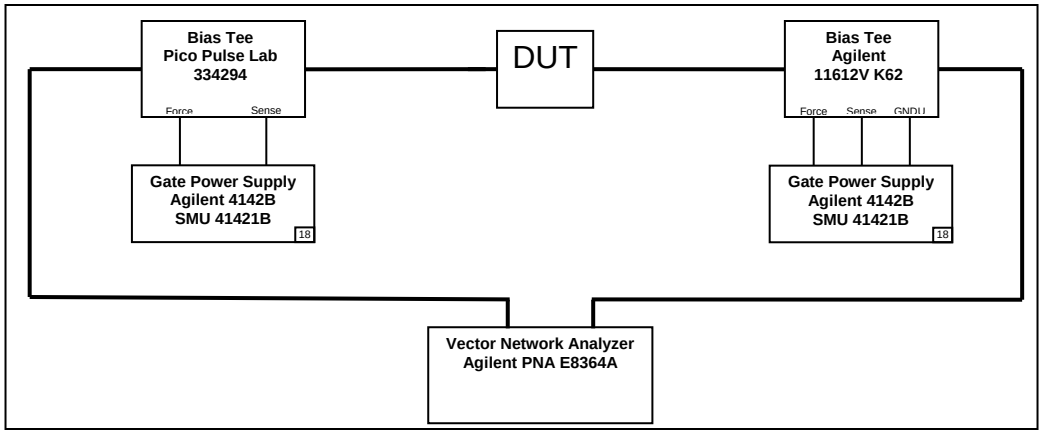


Figure 8. Block diagram of the cold FET measurement system.

In order to perform the required measurements for the cold FET test, the test system must be able to apply a bias to the device, measure the current, and measure the S-parameters. The bias controls the operating regime of the device under test (DUT). The current must be monitored in order to tell when the device is sufficiently forward biased so the diode junction is in the "on"

state. The S-parameters are used to measure the high frequency model of the device. In our setup, the voltage and current were both provided and measured by an HP4142B power supply. The S-parameters were measured using an Agilent E8364A.

The hardware is connected to a computer from where the instruments are externally controlled. We used the programs written for the scripting language program MATLAB to control the experiment and record the measurements. We recorded the data into a series of files, and then analyzed this data using different algorithms, as well as implemented the data in MATLAB and calculated and recorded the values for the parasitic elements.

### 3.2 Procedures

Prior to performing the experiment, we calibrated the Vector Network Analyzer (VNA) using the thru, reflect, line (TRL) calibration procedure. The DUT is placed on the test station and the probes are landed on the device.

The function that controls the instruments that perform the measurements during the cold FET test is *Measure_Gate_Data*.

The format for the function is as follows:

```
[Ig] = Measure_Gate_Data(Dev_name, Max_gate_power, Max_gate_V, Min_gate_V)
```

The inputs are as follows:

| | |
|---|---|
| Dev_name | (Text string) The device name is a text string that used is in generating the output files. |
| Max_gate_power | (Milliwatts, floating point decimal number) This is the maximum power that is allowed to pass through the device before the experiment is terminated. |
| Max_gate_V | (Volts, floating point decimal number) This is upper limit of the voltage sweep. |
| Min_gate_V | (Volts, floating point decimal number) This is lower limit of the voltage sweep. |

The outputs are as follows:

| | |
|---|---|
| Ig | (Milliamps, floating point decimal vector) This is a vector that consists of the gate current for each voltage measure. |

The function generates two types of output files:

- %Dev_name_VDS0.0_VGS#.#.s2p: This file records the measured S-parameters for a given bias in touchstone format.

- % Dev_name_Gate_IV.dcp: This file records the gate current and voltage of the device over the range of the voltage sweep.

An example usage of the function would take the following form:

```
[Ig] = Measure_Gate_Data('Dev_1_test_1', 0.1, 3, -5)
```

The function begins by biasing the device to the minimum voltage. The S-parameters at this bias are measured and recorded in a file. The voltage is increase incrementally. Once the voltage passes positive one volt, the program begins measuring and recording the forward bias S-parameter measurements. The sweep terminates when the DC power being dissipated exceeds the maximum power or when the voltage reaches the maximum voltage.

At the successful conclusion of the program, S-parameter files in touchstone format for different biases are written to the hard drive, and a file containing the current-voltage parameters is generated.

At this point the measurements are completed and the data must be analyzed. The S-parameters are uploaded into MATLAB and two separate functions are used to calculate the values of the parasitic elements of the DUT.

The first function has the format shown below and is used to compute the parasitic capacitances from the negatively biased S-parameters:

```
[Cpgd, Cpds, Cpgs] = extract_pad_cap(S,Start_freq,Stop_freq)
```

The inputs are as follows:

| | |
|---|---|
| S | (S-parameters, N×5 complex floating point decimal matrix) This input contains the S-parameters in touchstone format for the reversed biased DUT. |
| Start_freq | (GHz, floating point decimal) This is the lowest frequency in the S-parameters that is used in the calculations. |
| Stop_freq | (GHz, floating point decimal) This is the highest frequency in the S-parameters that is used in the calculations. |

The outputs are the parasitic capacitances:

| | |
|---|---|
| Cpgd | (Farads, floating point decimal) This is the gate drain parasitic capacitance. |
| Cpds | (Farads, floating point decimal) This is the drain source parasitic capacitance. |
| Cpgs | (Farads, floating point decimal) This is the gate source parasitic capacitance. |

An example usage of the function would take the following form:

```
[Cpgd, Cpds, Cpgs] = extract_pad_cap(S_pinch_off,.2,1);
```

The other function has the format shown below and is used to compute the parasitic capacitances from the negatively biased S-parameters:

```
[Rs, Rg, Rd, Ls, Lg, Ld] = extract_L_R(S,Start_freq,Stop_freq, Cpgd, Cpds,
Cpgs)
```

The inputs are as follows:

| | |
|---|---|
| S | (S-parameters, N×5 complex floating point decimal matrix) This input contains the S-parameters in touchstone format for the forward-biased DUT. |
| Start_freq | (GHz, floating point decimal) This is the lowest frequency in the S-parameters that is used in the calculations. |
| Stop_freq | (GHz, floating point decimal) This is the highest frequency in the S-parameters that is used in the calculations. |
| Cpgd | (Farads, floating point decimal) This is the gate drain parasitic capacitance. |
| Cpds | (Farads, floating point decimal) This is the drain source parasitic capacitance. |
| Cpgs | (Farads, floating point decimal) This is the gate source parasitic capacitance. |

The outputs are the series parasitic values:

| | |
|---|---|
| Rs | (Ohms, floating point decimal) This is the series source parasitic resistance. |
| Rg | (Ohms, floating point decimal) This is the series gate parasitic resistance. |
| Rd | (Ohms, floating point decimal) This is the series drain parasitic resistance. |
| Ls | (Henries, floating point decimal) This is the series source parasitic inductance. |
| Lg | (Henries, floating point decimal) This is the series gate parasitic inductance. |
| Ld | (Henries, floating point decimal) This is the series drain parasitic inductance. |

An example usage of the function would take the following form:

```
[Rs, Rg, Rd, Ls, Lg, Ld] = extract_L_R(S_forward, 20,38, Cpgd, Cpds, Cpgs);
```

These functions calculate the parasitic parameter values in the manner described in section 2.

## 4. Results

The procedure was performed on a number of devices. The values of the components in the equivalent circuit model were extracted and S-parameters for the equivalent circuit model were calculated. A representative example of these calculations is presented. We used Agilent's Advanced Design System (ADS) computer aided design program to compare measured data with modeled data. Figure 9 shows the circuit used to compare the reverse bias measured data with the modeled data.

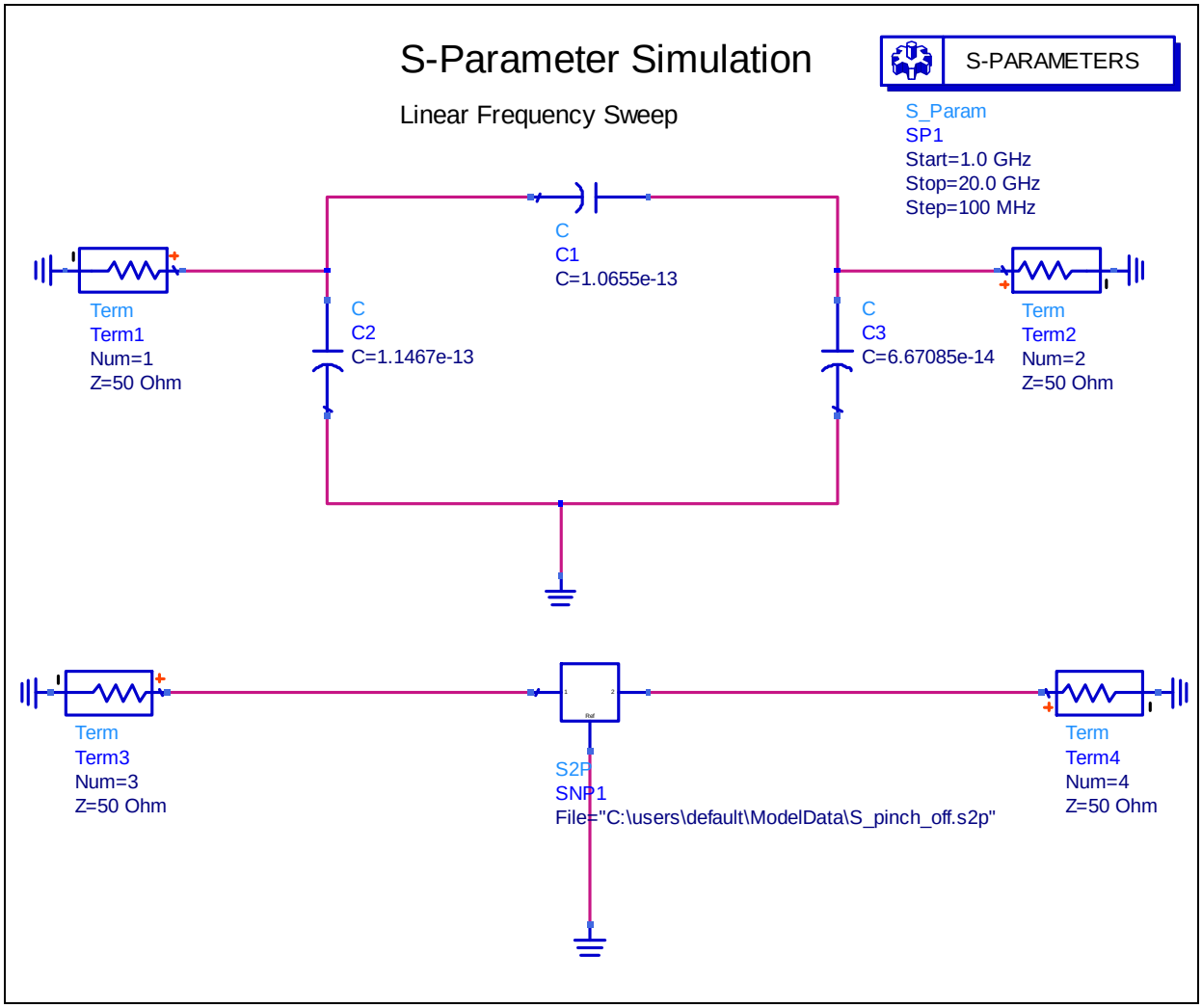


Figure 9. ADS circuit used to compare measured data with the model for the reverse biased device.

Figure 10 shows the comparison of the measured and modeled data from 1 to 20 GHz.

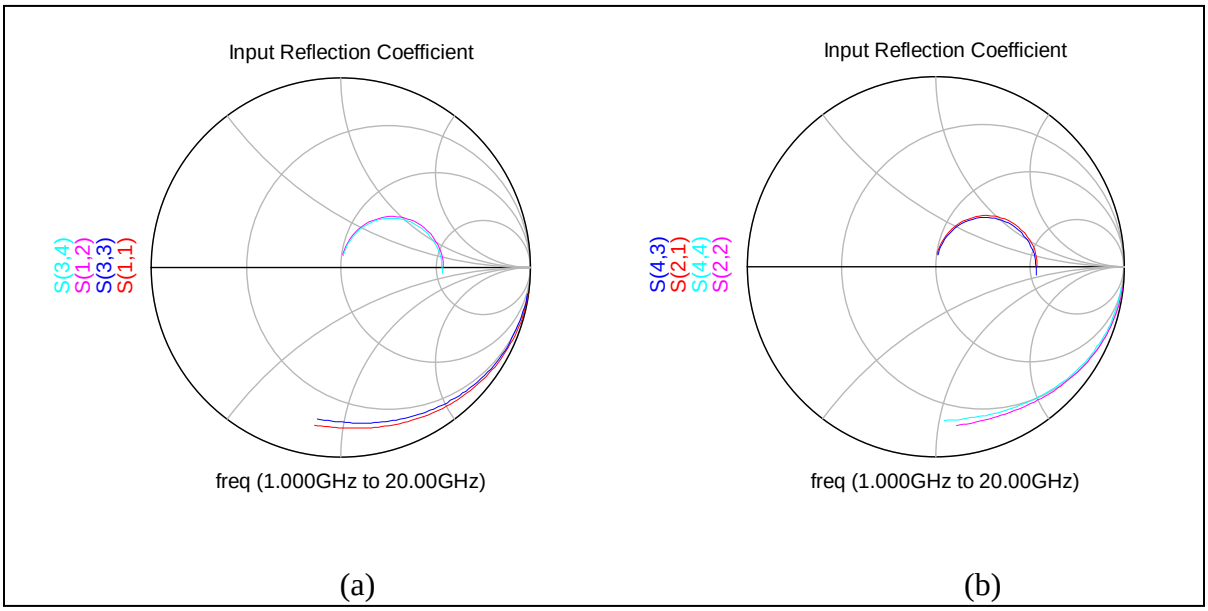


Figure 10. Reverse biased measured and modeled S-parameters compared (a) $S_{11}$ and $S_{12}$ and (b) $S_{22}$ and $S_{21}$.

Note: The lower numbered (1,2) S-parameters are modeled and higher numbers (3,4) are measured.

The circuit used to model the forward-biased devise is shown in figure 11.

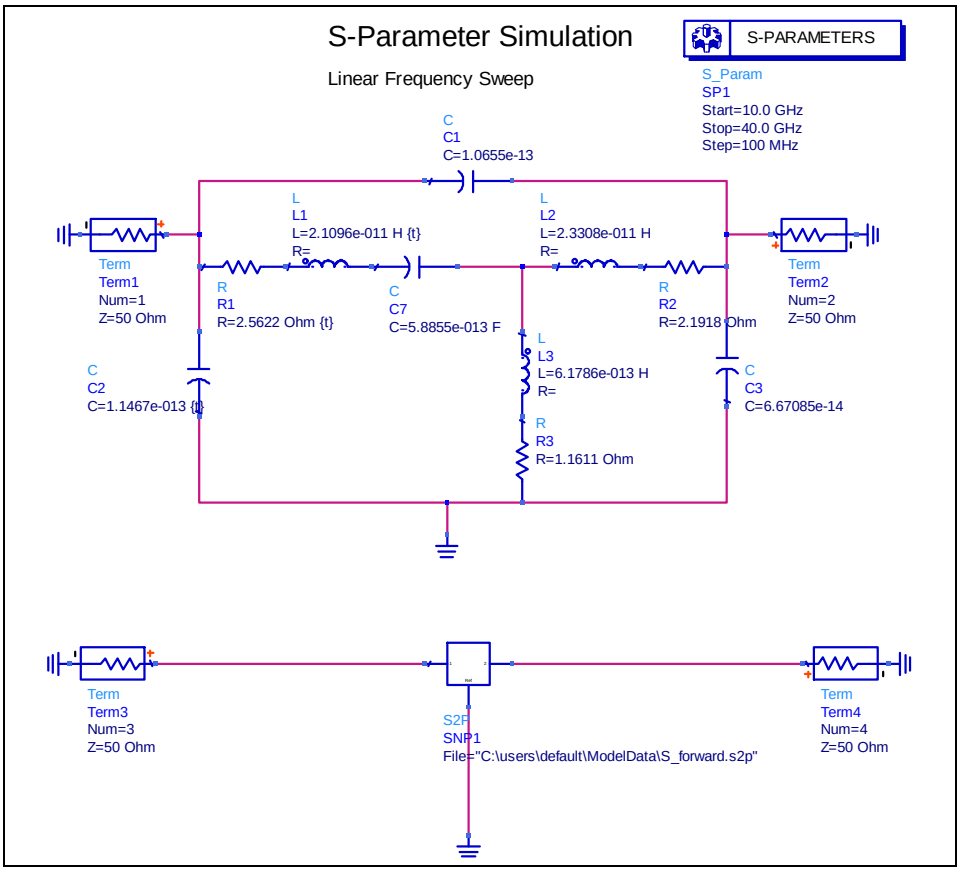


Figure 11. ADS circuit used to compare measured data with the model for the forward-biased device.

The measured S-parameters for the forward-biased device are compared to those of the modeled device in figure 12 from 10 to 40 GHz. The frequency ranges shown in figures 10 and 12 were selected to be where the parasitics being measured would have the largest effect. These are low frequencies for capacitors and high frequencies for inductors.

We calculated the error by taking the absolute value of the difference between measured and calculated values divided by the absolute value of the measured value. The average error for $S_{11}$ and $S_{22}$ for the reverse bias model was less than 6%. The error for the $S_{11}$ and $S_{22}$ for the forward bias model was less than 7%. The forward and reverse transmission parameters ($S_{12}$ and $S_{21}$) were higher but on average less than 15%. The magnitude of the transmission parameters was much smaller than the reflection coefficients. This aspect makes them more susceptible to measurement errors. These errors are from the directly extracted values, and we have successfully reduced these values by using optimization algorithms. Optimizing the parasitic elements together with the small-signal model of the device resulted in errors of less than a few percent.

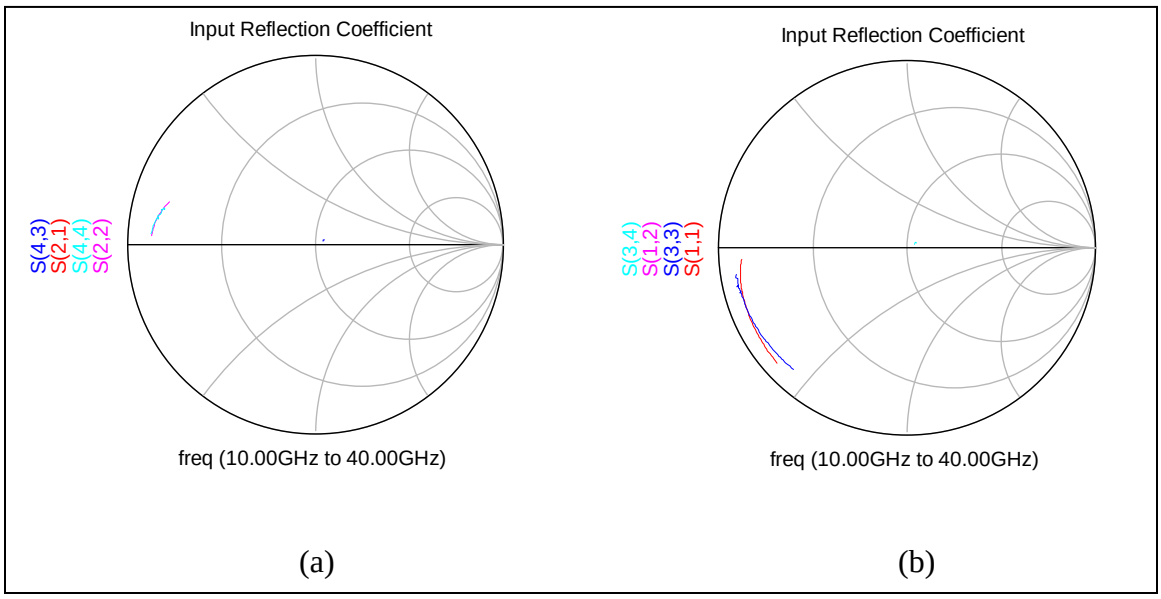


Figure 12. Forward biased measured and modeled S-parameters compared (a) $S_{22}$ and $S_{21}$ (b) $S_{11}$ and $S_{12}$.

Note: The lower numbered (1,2) S-parameters are modeled and higher numbers (3,4) are measured.

## 5. Conclusions

The ability to isolate and determine the parasitic capacitances of a device under test is a crucial step in generating either small-signal or large-signal device models. We have implemented a well-known parasitic extraction algorithm that determines the component values of a device model that reliably reproduce the measured data. Our technique builds upon existing parasitic

extraction algorithms by numerically determining the residual intrinsic device gate capacitances. This technique has been fully automated and can be integrated into other model generation procedures.

The software used to perform the measurements and calculations describe in the report is available upon request for use in the interest of the Government on a case-by-case basis as determined by the authors.

## 6. References


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